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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/663,304
Filing Date: September 16, 2003
Appellant(s): BERA ET AL.

Alan Taboada
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 22,2007 appealing from the Office actions mailed 08/31/2006 and 06/01/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes according the Advisory Action mailed 08/31/2006 are as follows:

Claims 1-6, 8-10 and 40-43 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. US 6,797,633 B2 in combination with Ikeda US 6,426,299 B1.

Claims 7 and 11-17, 44-45 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in combination with Ikeda as applied to claims 1-6, 8-10

and 40-43 above, and further in view of Chun et al. TW 544815 A and Samukawa et al. US 6,177,146 B1.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,797,633 B2	Jiang et al.	9-2004
6,426,299 B1	Ikeda	7-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-6, 8-10 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. US 6,797,633 B2 in combination with Ikeda US 6,426,299 B1.

Re claim 1 and 40, the Jiang et al. reference discloses a method of fabricating an interconnect structure, which "may be the first or any subsequent metal interconnect level of the semiconductor device 120" (col. 3, lines 24-26, i.e., the disclosed process is considered to start on the formed structure of fig. 1F), comprising:

(a) providing (first metal interconnect level of the semiconductor device 120 being formed with) a substrate 100 having a film stack comprising sequentially formed on the substrate a first barrier layer 101, a conductive layer 124 embedded in a first dielectric layer 102/104, fig. 1F, (subsequent metal interconnect level of the semiconductor device 120 being formed with) a second barrier layer 101, a second dielectric layer 102/104,

and a cap layer 105 (fig. 1A, the considered substrate 100 in this figure is the formed first metal interconnect level of fig. 1F);

(b) etching a via hole 106 in the cap layer and the second dielectric layer 102/104 (fig. 1C);

(c) filling a portion of a depth of the via hole with a masking material 107 (fig 1D);

(d) etching in-situ the cap layer 105, a trench 108 in the second dielectric layer 102/104, the masking material 107 (fig. 1E), and the second barrier layer 101(fig. 1F); and

(e) metallizing the via hole and the trench (fig. 1F).

The Jiang et al. reference *discloses* substantially all of the steps of the instant invention, teaches O_2 plasma and other chemistries are provided with or without inert gases to treat low-k films without damage to the OSG film (col. 3, lines 45-67) "[t]he exposure energy (*power*) required to clear resist inside a via is the lowest for the wafer with in-situ O_2 plasma ash, indicating the most robustness for fighting poisoning" (col. 4, lines 15-26).

The Jiang et al. reference *lacks* providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of the etching period (re claim 1, step d) *or while etching the dielectric layer* (re claim 40, step c).

The Ikeda reference discloses a method of etching the structure of fig.3 wherein a SiON 103, a SiO_2 104, an organic ARC 105 and a photoresist pattern 106 formed in that sequence on the base 101 with plug 102 embedded to reduce the F radicals (col. 1,

lines 28-29 and col. 2, lines 35-37). The method in fig. 4 discloses plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of etching period and/or *while etching a dielectric layer* (at least at step II, e.g.).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the sub-steps of Jiang et al. with the power, pressure and flow rates as taught by Ikeda *to provide a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts* while etching *during at least a portion of etching period according to the choice of gases and energy/power as suggested by* Ikeda because the power, pressure and flow rates as suggested/taught by Ikeda would provide the sub-steps of Jiang et al. with reducing the F radicals which form a hardened surface layer.

Re claim 2, the Jiang et al. reference teaches wherein the cap layer comprises SiO_xN_y, where x and y are integers (col. 3, line 40).

Re claims 3 and 41, the Jiang et al. reference teaches wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass (col. 3, lines 28-36).

Re claim 4, the Jiang et al. reference teaches wherein the first barrier layer and the second barrier layer comprise at least one of SiO_2, SiC and Si_3N_4 (col. 1, line 52).

Re claim 5, the Jiang et al. reference teaches wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN and TiN (col. 2, line 41).

Re claim 6, the Jiang et al. reference teaches wherein the masking material is selected from a group consisting of an organic material and photoresist (col. 4, lines 9-14).

Re claim 8, the Jiang et al. reference teaches wherein the step (c) further comprises: applying the masking material 107 to the substrate to fill the via hole 106; and etching back the masking material 107 until the masking material is removed from the via hole to a pre-determined depth that is smaller than a depth of the trench (col. 4, lines 9-15).

Re claims 9 and 42-43, the Jiang et al. reference teaches wherein the etching step further comprises: providing O_2 at a flow rate from about 100 to 1000 sccm; maintaining a chamber pressure at about 5 to 200 mTorr; and applying a cathode bias power between 100 and 400 W (col. 3, lines 1-4).

Re claim 10, the Jiang et al. reference teaches wherein the step (d) further comprises: forming on the cap layer a second patterned etch mask 132 to define the trench 108; and stripping the second patterned etch mask 132 contemporaneously with etching the masking material (col. 4, lines 27-30).

2. Claims 7 and 11-17, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in combination with Ikeda as applied to claims 1-6, 8-10 and 40-43 above, and further in view of Chun et al. TW 544815 A and Samukawa et al. US 6,177,146 B1.

Although the Jiang et al. reference discloses in the step (b): forming a first patterned etch mask 130 on the cap layer 105 to defined via hole 106; etching the via hole; and stripping the first patterned etch mask (figs. 1C and 1D), *re claim 7*; and in step (d): "[t]rench pattern 132 and BARC 107 are then removed. The capping layer 105 and etchstop layer 101 are removed next during and etchstop etch" (col. 4, lines 28-30); the Jiang et al. reference discloses without details of VHF frequency, bias power at a frequency, or source power and the ratio of CF_4:N_2 in each sub-step, *re claims 11-17 and 44-45*. The combination teaches substantially all of the instant invention, the combination still lacks the ratio of CF_4:N_2 in a range from 1:1 to 1:5 in forming the via hole and an indication of the frequency of the VHF while etching.

The Chun et al. reference teaches etching through a cap layer on the dielectric layer using N_2 and CF_4 in the ratio of 0-10:1.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the via hole etching of the combination with the ratio of CF_4:N_2 as taught by Chun et al. because that ratio of Chun et al. would improve the etching rate of nitride to oxide layer as taught by Jiang et al.

And Samukawa et al. teaches that etching by exposing to plasma has been widely applied since it is highly practicable. High-density plasma etching generated in the course of electric discharge caused by applying an electric field of high frequency ranging in VHF to UHF bands, nearly from 100 to 1,000 MHz (col. 1, lines 20-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of the combination with an appropriate VHF frequency

as taught by Samukawa et al. because the frequency of Samukawa et al. would provide the method of the combination with highly practicable. The use of frequency ranging in VHF to UHF bands in plasma etching is well known to those skill in the art as taught by Samukawa et al.

(10) Response to Argument

First of all, appellant's arguments related to Maa et al. are moot in view of the Advisory Action mailed 08/31/2006 in which the rejection(s) based on Maa et al. is(are) withdrawn.

It is agreed that the Jiang et al. reference lacks providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of the etching period *or while etching the dielectric layer.* However, the Ikeda reference discloses, in fig. 4, step II, e.g., plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts *while etching* during at least a portion of etching period and/or *while etching a dielectric layer* (not as alleged as in the Argument).

In response to appellant's argument on pages 6-7 that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case,

the Jiang et al. reference discloses substantially all of the steps of the instant invention without providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of step (d); it would have been obvious to employ the process conditions of Ikeda, including those of step II, for the process of Jiang to enable the disclosed silicon oxide ILD etching step of Jiang to be performed according to the teachings of Ikeda because Ikeda discloses the conditions are useful in etching stacked layers in the formation of a damascene structure. The fact that Ikeda discloses additional structure//limitation of sputtered Si, which is not claimed, is irrelevant. Further, grounding upper electrode only happens in step III when the first interlayer and the hardened layer being removed/etched away.

In response to appellant's argument that "the Examiner's rebuttal inappropriately presumes the combination" referring Office Actions dated 11/22/2005 and 02/24/2006, this argument is not timely response. The examiner believes those rebuttals are proper to the instances at the time.

In response to appellant's arguments at the end of page 7 and pages 8-9, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985). Further, in response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account

only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The instant claimed invention is the combination of many etching steps onto many different layers for a dual damascene interconnection structure formation. The examiner takes initial burden to analyze the claim and applies prior art to each step in the instant claimed invention. The objective teachings of prior art go along with the many steps in the combination. The reasons for the combinations are stated. The tests for obviousness are also provided.

In response to appellant's arguments in Section 2 of the Argument, neither Jiang nor Chun nor Samukawa is used for the source and bias power, Ikeda is.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Thanh V. Pham

Conferees:

Matthew Smith

David Blum